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Article

A New Mirroring Circuit for Power MOS Current Sensing Highly Immune to EMI

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Abstract: This paper deals with the monitoring of power transistor current subjected to radio-frequency interference. In particular, a new current sensor with no connection to the power transistor drain and with improved performance with respect to the existing current-sensing schemes is presented. The operation of the above mentioned current sensor is discussed referring to time-domain computer simulations. The susceptibility of the proposed circuit to radio-frequency interference is evaluated through time-domain computer simulations and the results are compared with those obtained for a conventional integrated current sensor.

Keywords: current sensor; CMOS integrated circuit; smart power; electromagnetic interference (EMI); electromagnetic compatibility (EMC); senseFET; miller effect

1. Introduction

In the last decades, the development of CMOS technologies in terms of scale integration and component performance has made the integration of full electronic system into a single chip possible. Such System-on-Chips (SoCs) comprise complex high-speed digital blocks, analog circuits and power section [1,2]. The power-supply voltage of such integrated circuits has decreased over time, leading to lower noise margins. However, the level of disturbances collected by the wiring harnesses of the

electronic systems from the surrounding environment has strongly increased because of the widespread use of wireless systems for radio/TV broadcasting and mobile communications. In this context, the need to understand the effect of radio frequency interference (RFI) on baseband integrated circuits has continued to grow and several studies have tried to set out design guidelines and new circuit topologies for making integrated circuits immune to RFI [3–8]. Such disturbances superimposed onto nominal signals are of particular concern in the design of input and output front-end integrated circuits like those included in smart power ICs, which cannot be protected using EMI-filters at the PCB level because either their presence can affect the nominal circuit operation or the PCB is not present since the SoC is encapsulated inside the sensor (actuator) plastic holder. For instance, EMI filters and capacitors cannot be connected to the power transistor terminals because they would reduce the power efficiency. As a result, the power transistors that drive actuators through cables can experience high-level RFI that can lead to unexpected transistor switching and leakage currents, as shown in [9,10]. In addition to this problem, the circuits that are connected to the transistors' terminals, including circuits embedded in smart power ICs for monitoring the operation of the power transistors and the actuators, are also affected by RFI.

Within the aforementioned context, this paper investigates the susceptibility of integrated current sensors that are used in power circuits for control and/or safety purposes to RFI. The current of a power transistor can be sensed by using one of the circuits presented in [11], but only a few of them are suitable for integration on silicon. Among these integrated current sensors, one of the most frequently used is that based on a small transistor namely SenseFET. The voltages at the terminals of the SenseFET are kept equal to those of a power transistor in which the current to be detected flows. In this way, such a current is scaled by a constant K and provided by the SenseFET. K depends only on the aspect ratios $\left(\frac{W}{L}\right)$ of the two transistors. In this circuit, the SenseFET is electrically connected to the terminals of the power transistor and therefore it is affected by the RF disturbances collected by cables. In order to design embedded current sensor immune to such RF interferences, this paper presents a new integrated current-sensing solution conceived to be electrically not connected to the power transistor drain that can be affected by disturbances. The current is sensed whenever during its transient the power transistor and the SenseFET both operate in saturation. Therefore, the current flowing through the power transistor is mirrored by the SenseFET, is not dependent on the drain-source voltage and is only related with the mirroring factor K. The paper is organized as follows. Section 2 describes the operation of a common integrated current sensor. Section 3 summarizes the switching behavior of power MOSFETs. On the basis of such a behavior, a new current sensor not electrically connected to the drain terminal of the power transistor is proposed in Section 4. Then, the results of computer simulations aimed at evaluating the susceptibility of the proposed current sensor, the MagFET-based sensor and the commonly used current sensor to RFI are shown in Section 5. Finally, some concluding remarks are drawn in Section 6.

2. A Conventional Current Sensor: The SenseFET

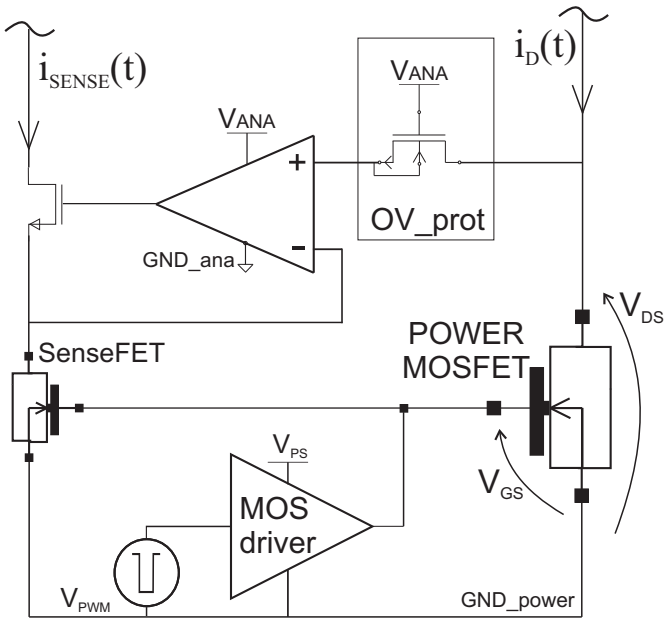
Common current sensors for integrated applications are based on the SenseFET circuit topology, in which the current $i_{\mathrm{D}}(t)$ that flows through an MOS Power transistor is sensed using an elementary transistor of the same type that is used in the power transistor. Figure 1 shows the operation of the

SenseFET current sensor, where the gate terminals of the aforementioned transistors are connected to each other and driven by an MOS driver, while the drain-to-source voltage of the SenseFET is made equal to that of the power transistor by means of a voltage follower. In this circuit, the relationship between the power transistor current (I_{D}) and the sensed current (I_{SENSE}) can be written as

$$K = \frac{\left(\frac{W}{L}\right)_{\mathrm{power}}}{\left(\frac{W}{L}\right)_{\mathrm{sense}}} \tag{1}$$

where $\left(\frac{W}{L}\right)_{\mathrm{power}}$ and $\left(\frac{W}{L}\right)_{\mathrm{sense}}$ are the aspect ratios of the power and SenseFET transistors, respectively. K is typically not lower than 10^3. The scaled current I_{SENSE} is then converted to a voltage, using a resistor to be used for digital signal processing. This paper focuses on a low side sensing topology highlighted in Figure 1.

Figure 1. Current sensor based on the SenseFET technique.



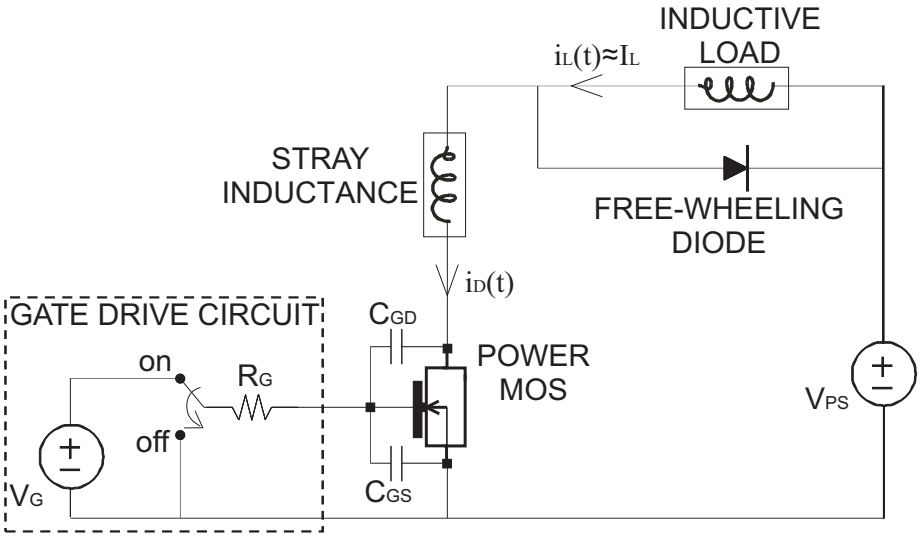
However, the same reasoning can be applied for the high side topologies. In this technique the power dissipation is low and the accuracy is related to the matching of the SenseFET and the Power MOS. The two transistors are driven in the deep triode region by the same gate-source voltage and have to be kept at the same drain-source voltages. Therefore, to minimize the error in the sensed current, the amplifier needs to have a very high gain. Moreover, the amplifier should maintain the accuracy across the large input common-mode range. Although several circuit topologies of current sensors have been proposed, all of them include an amplifier, which implies stability issues, limited bandwidth and increased design complexity. In fact, the improvements in integrated current-sensing are basically focused on increasing amplifier performance [12–19]. Furthermore, the presence of the amplifier increases the overall susceptibility of the commonly employed SenseFET-based current sensing to EMI. In fact, this amplifier is connected through an over-voltage protection (see Figure 1) to the power transistor drain, and hence to the wiring interconnects at the system level that collect EMI. Since interference with an amplitude of hundreds of mV causes distortion in the amplifier and in the over-voltage protection, the operation of the current sensor can be impaired [6].

For all the above mentioned reasons, a new current sensor with improved performance due to the absence of any amplifier has been designed and its immunity to EMI is specifically addressed in this paper.

3. Power MOSFET Switching Characteristics

The Power MOSFET is usually employed as a switch in circuits for energy conversion and management applications and to drive high-power loads. For instance, a Power MOSFET is used to control the current in inductive loads such as the windings of motors. A Power MOSFET that drives an inductive load is represented in Figure 2 where a freewheeling diode carries the load current when the Power MOS is switched-off and a stray inductance is included to account for package and board parasitic elements.

Figure 2. Power MOSFET device operating in an inductive load circuit.



The switching behavior of Power MOSFET structures is governed by the gate drive circuit and the nature of the load. The power transistor is switched on and off by a control or gate drive circuit, which can be represented (Thevenin's equivalent) as a DC voltage V_{G} with a series resistance R_{G}. The load current i_{L} transfers between the power MOSFET device and the freewheeling diode during each operating cycle. The inductor is charged and its current is increased when the Power MOSFET is turned-on while it is discharged when the load current flows through the diode. However, the change in the inductor current is small during one cycle, allowing the assumption that the current I_{L} is constant. On the basis of that, a new current sensor that operates during the transient of the Power MOSFET has been conceived. To this purpose, the waveform of the transient of a Power MOSFET is represented in Figure 3 and described in the following. Whenever the Power MOSFET is in off-state, the load current flows through the freewheeling diode. The initial conditions for the Power MOSFET are defined by $v_{\mathrm{GS}}(0) = 0$, $i_{\mathrm{D}}(0) = 0$, $v_{\mathrm{DS}}(0) = V_{\mathrm{DS_{OFF}}}$. During the turn-on process, the gate bias voltage source V_{G} starts to charge the capacitances of the Power MOSFET. Since no drain current can flow through the power MOSFET device until the gate voltage exceeds its threshold voltage, the drain voltage initially remains

at the drain bias voltage. The gate–drain capacitance $C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})$ remains constant because the drain voltage is constant. Consequently, the time constant for charging the gate of the power MOSFET device is $R_{\mathrm{G}} \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})]$, resulting in a gate voltage given by

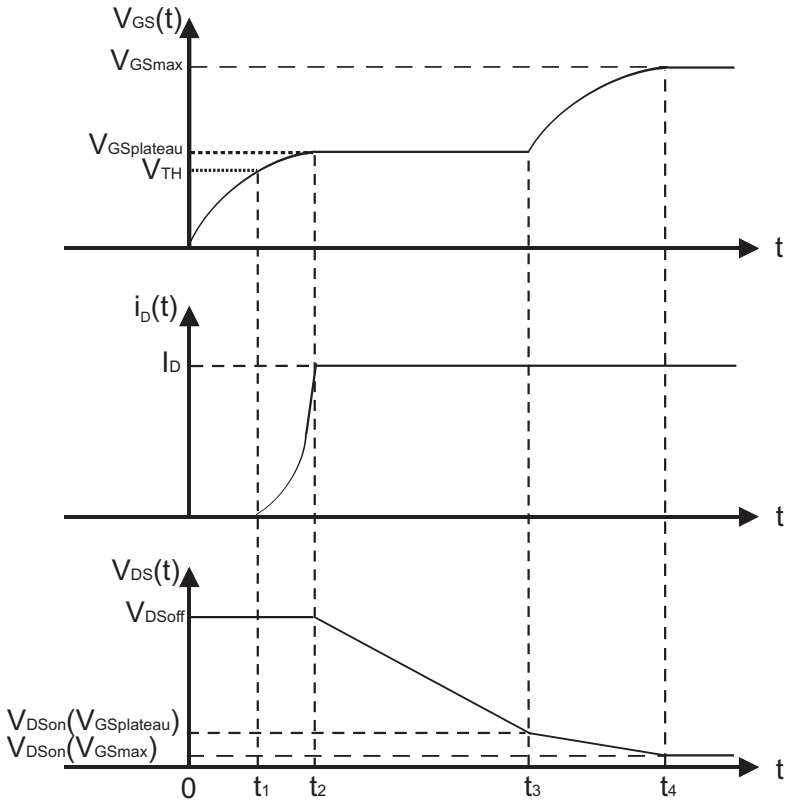
$$v_{\mathrm{GS}}(t) = V_{\mathrm{GS_{max}}} \cdot \left[1 - e^{-\frac{t}{R_{\mathrm{G}} \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})]}}\right] \tag{2}$$

and represented in Figure 3. The gate voltage reaches the threshold voltage at time t_1:

$$v_{\mathrm{GS}}(t)|_{\mathrm{t=t_1}} = V_{\mathrm{TH}} \tag{3}$$

$$t_1 = R_{\mathrm{G}} \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})] \cdot ln\left(\frac{V_{\mathrm{GS_{max}}}}{V_{\mathrm{GS_{max}}} - V_{\mathrm{TH}}}\right) \tag{4}$$

Figure 3. Waveforms for the power MOSFET during turn-on with a gate voltage source.



Once the gate voltage exceeds the threshold voltage, drain current begins to flow.

$$i_{\mathrm{D}}(t) = \frac{\mu_{\mathrm{ni}} C_{\mathrm{OX}} W_{\mathrm{CH}}}{L_{\mathrm{CH}}} \cdot [v_{\mathrm{GS}}(t) - V_{\mathrm{TH}}]^2 \tag{5}$$

Although the drain current increases, the drain voltage remains at the drain supply voltage $V_{\mathrm{DS_{OFF}}}$ because the diode cannot sustain any voltage until all of the load current is transferred to the Power MOSFET. Since the drain voltage remains constant, the drain–gate capacitance is also invariant in the range $[t_1 - t_2]$. Consequently, the gate voltage continues to increase at an exponential rate as described

by Equation (2) with the same time constant. The drain current increases as the square of the gate voltage as described by Equation (5) with a nonlinear waveform as represented in Figure 3.

The drain current increases until it becomes equal to the load current $I_{\mathrm{D}} = I_{\mathrm{L}}$ and $v_{\mathrm{GS}}(t)$ reaches the voltage plateau $V_{\mathrm{GS_{plateau}}}$ at the time t_2.

$$v_{\mathrm{GS}}(t)|_{\mathrm{t=t_2}} = V_{\mathrm{GS_{plateau}}} = V_{\mathrm{GS_{max}}} \cdot \left[1 - e^{-\frac{t_2}{R_{\mathrm{G}} \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})]}}\right] \tag{6}$$

$$t_2 = R_{\mathrm{G}} \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS_{OFF}}})] \cdot ln\left(\frac{V_{\mathrm{GS_{max}}}}{V_{\mathrm{GS_{max}}} - \sqrt{\frac{I_{\mathrm{D}} L_{\mathrm{CH}}}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W_{\mathrm{CH}}}} - V_{\mathrm{TH}}}\right). \tag{7}$$

All of the load current has transferred from the diode to the Power MOSFET device at time t_2 and the diode is now able to support voltage. The drain-source voltage of the Power MOSFET starts to reduce at this time. Since the drain current is constant and equal to the load current ($I_{\mathrm{D}} = I_{\mathrm{L}}$), the gate voltage at time t_2 can be also expressed as

$$v_{\mathrm{GS}}(t)|_{\mathrm{t_2-t_3}} = V_{\mathrm{GS_{plateau}}} = V_{\mathrm{TH}} + \sqrt{\frac{I_{\mathrm{D}} L_{\mathrm{CH}}}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W_{\mathrm{CH}}}}. \tag{8}$$

The gate-source voltage remains constant at the plateau voltage until the drain-source voltage has reduced to the on-state voltage drop corresponding to the product of the load current and the on-resistance of the device at a gate bias equal to the plateau voltage. Since the gate voltage is constant during the plateau phase, all the gate current $i_{\mathrm{G_{plateau}}}$ is used to charge the gate–drain or Miller capacitance. The gate current during the plateau phase is given by

$$i_{\mathrm{G_{plateau}}} = \frac{V_{\mathrm{GS_{max}}} - V_{\mathrm{GS_{plateau}}}}{R_{\mathrm{G}}}. \tag{9}$$

As this current charges the gate–drain capacitance, its voltage decreases at a rate given by

$$\frac{dv_{\mathrm{GD}}(t)}{dt} = -\frac{i_{\mathrm{GP}}(t)}{C_{\mathrm{GD}}(v_{\mathrm{DS}}(t))}. \tag{10}$$

Since the gate–source voltage is constant at $V_{\mathrm{GS_{plateau}}}$ during this time, the drain voltage also decreases linearly with time:

$$\frac{dv_{\mathrm{DS}}(t)}{dt} = \frac{dv_{\mathrm{GD}}(t)}{dt} = -\frac{i_{\mathrm{GP}}(t)}{C_{\mathrm{GD}}(v_{\mathrm{DS}}(t))} = -\frac{V_{\mathrm{GS_{max}}} - V_{\mathrm{GS_{plateau}}}}{R_{\mathrm{G}} \cdot C_{\mathrm{GD}}(v_{\mathrm{DS}}(t))}. \tag{11}$$

At the end of the plateau phase at time t_3, the drain–source voltage becomes equal to the on-state voltage drop corresponding to the plateau gate bias voltage. Based on this, the duration of the plateau can be expressed as:

$$\int_{t_2}^{t_3} dv_{\mathrm{D}} = \int_{t_2}^{t_3} -\frac{V_{\mathrm{GS_{max}}} - V_{\mathrm{GS_{plateau}}}}{R_{\mathrm{G}} \cdot C_{\mathrm{GD}}(v_{\mathrm{DS}}(t))}\, dt \tag{12}$$

$$t_3 - t_2 = \frac{R_{\mathrm{G}} \cdot C_{\mathrm{GD_{AVG}}}}{V_{\mathrm{GS_{max}}} - V_{\mathrm{GS_{plateau}}}} \cdot [V_{\mathrm{DS_{OFF}}} - I_{\mathrm{D}} R_{\mathrm{DS_{ON}}}(V_{\mathrm{GS_{plateau}}})] \tag{13}$$

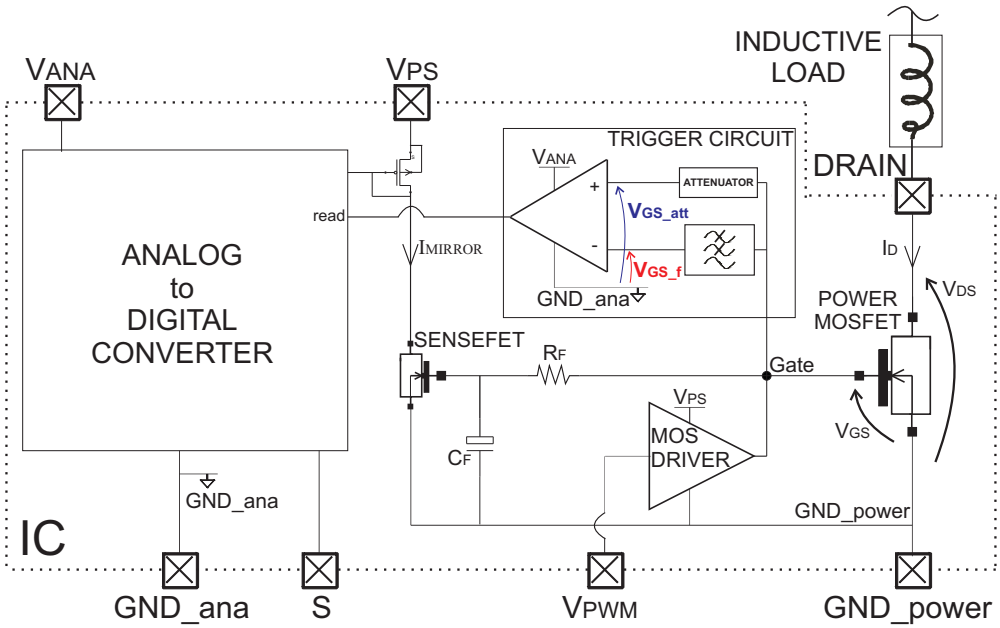
where $C_{\mathrm{GD_{av}}}$ is the gate–drain capacitance assumed to have a constant average value during the transient and $R_{\mathrm{DS_{ON}}}(V_{\mathrm{GS_{plateau}}})$ is the on-resistance of the power MOSFET device for a gate-source voltage equal to the plateau voltage. Beyond the plateau, the gate voltage increases exponentially again as shown in the Figure 3 until it reaches the gate supply voltage. The time constant for this exponential rise is different from the initial phase due to the large gate–drain capacitance. The increasing gate voltage produces a reduction of the on-resistance of the power MOSFET device, resulting in a small reduction of the drain voltage during this fourth phase of the turn-on process.

Considering reasonable value for the parasitics of the Power transistor sized in the order of mm^2 and for the integrated driving resistance R_{G}, the interval time $(t_3 - t_2)$ results to be larger than hundreds of nanoseconds. On the basis of a trigger event occurring during this interval, a new current sensor is proposed in Section 4.

4. A New Current Sensor Based on the Miller Effect

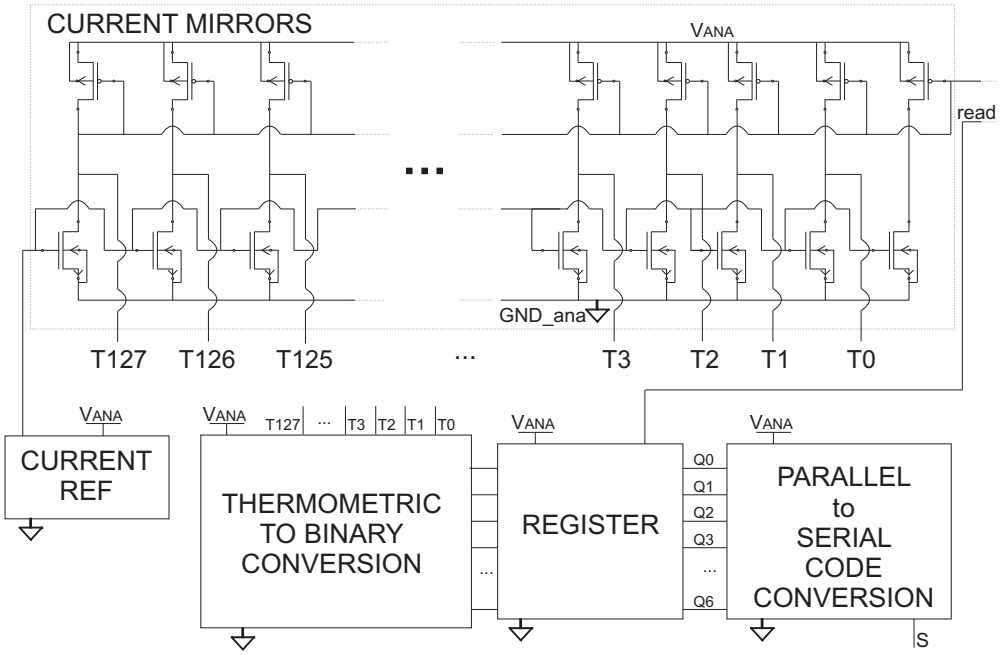
In order to design a current sensor immune to EMI, a new circuit is conceived, which is not electrically connected with the Power MOSFET drain terminal that is prone to disturbances. To this purpose, the current that flows through the Power MOSFET (i_{D}) is mirrored and processed during the V_{GS} voltage plateau due to the Miller effect (between points 2 and 3 in Figure 3). In this region, the Power MOSFET operates in the saturation region and the mirrored current I_{MIRROR} is not dependent on the drain-source voltage and is only related with the mirroring factor K. The Power MOSFET is driven by a PWM signal that provides both the proper-timing driving voltage and a negative pulse that generates a switching transient with negligible reduction of the current in inductive loads.

Figure 4. Block diagram of the proposed current sensor that exploits the Miller effect.



The block diagram of the proposed current sensor is shown in Figure 4. A low-pass RC filter ($R_{\mathrm{F}}-C_{\mathrm{F}}$) with a cut-off frequency significantly lower than the frequency of the EMI disturbances is placed between the Power MOSFET and SenseFET gates. In particular, $R_{\mathrm{F}} = 10\ k\Omega$ and $C_{\mathrm{F}} = 2\ pF$, so that the cut-off frequency is less than 10 MHz ($f_{\mathrm{CUT_OFF}} \approx 8\ MHz$). The current I_{unknown} is mirrored by a SenseFET, processed and converted in a serial code (Analog to Digital Converter in Figure 4, further reported in Figure 5). The SenseFET current, in turn, is mirrored 128 times. Each of these currents is compared with progressively scaled current references in order to provide a thermometric digital code of the SenseFET current I_{MIRROR}. Then, a further thermometric-to-binary conversion is provided [20]. As soon as a trigger event occurs, the binary code is written in a register. Such a binary word provides the value of the current to detect I_{unknown}, which is then converted to a serial code.

Figure 5. Analog to Digital Converter in Figure 4.



The trigger circuit is based on the comparison of an attenuated gate-source characteristic $V_{\mathrm{GS_{att}}}$ with the gate-source voltage after a low-pass filtering process $V_{\mathrm{GS_f}}$. Both these two voltages are obtained from the gate-source voltage V_{GS} by means of only passive component as represented in Figure 6. An inverting stage made of a high voltage inverter allows to null the current dissipation whenever the V_{GS} voltage transient ends. Neglecting the drop voltage across the transistor M_{SD} that operates in triode during the transient, the voltage $V_{\mathrm{GS_att}}$ is given by:

$$V_{\mathrm{GS_att}} = \frac{R_2(1+sR_1C_1)}{R_2(1+sR_1C_1)+R_1(1+sR_2C_2)}V_{\mathrm{GS}} \tag{14}$$

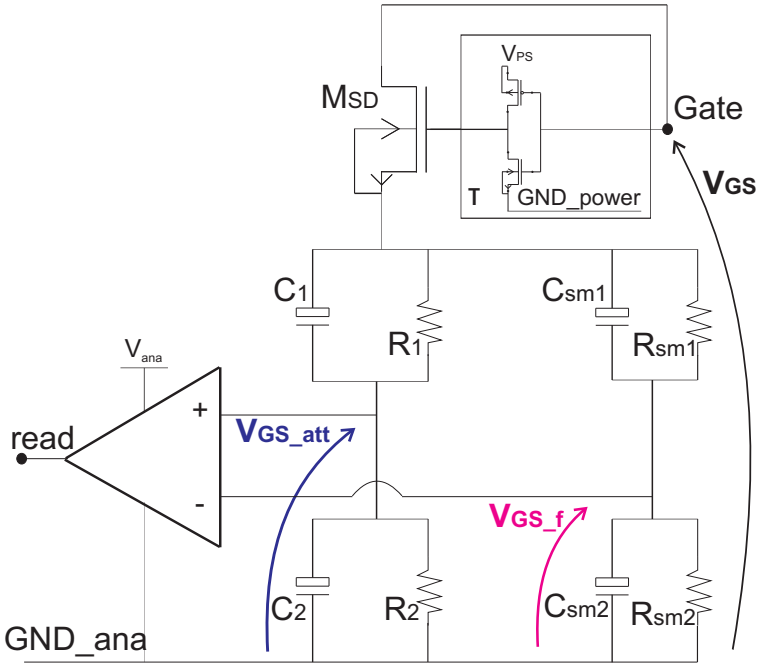
Setting $R_1C_1 = R_2C_2$ the voltage $V_{\mathrm{GS_{att}}}$ is simply the gate-source voltage V_{GS} scaled by a factor k_{din_adp} independently by the frequency components of the switching transient of the Power MOSFET.

$$V_{\mathrm{GS_att}} = \frac{R_2}{R_1+R_2}V_{\mathrm{GS}} = \frac{C_1}{C_1+C_2}V_{\mathrm{GS}} = k_{din_adp}\cdot V_{\mathrm{GS}} \tag{15}$$

where k_{din_adp} is set in order to not overcome the maximum voltage deliverable to the analog blocks.

$$k_{din_adp} = \frac{R_2}{R_1 + R_2} = \frac{C_1}{C_1 + C_2} \tag{16}$$

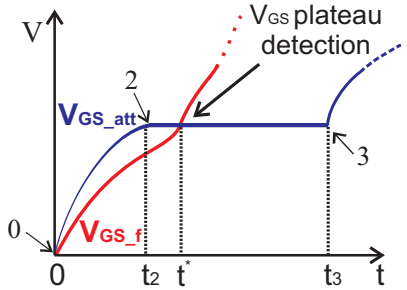
Figure 6. Trigger circuit.



The voltage $V_{\mathrm{GS_f}}$ is obtained by a filtering and the passive components (R_{sm1}, C_{sm1}, R_{sm2} and C_{sm2}) are set to makes this voltage $V_{\mathrm{GS_f}}$ lower than the attenuated voltage $V_{\mathrm{GS_{att}}}$ during the interval $[0 - t_1]$. At the same time, the passive components are set such that the filtered voltage $V_{\mathrm{GS_f}}$ reaches the attenuated voltage $V_{\mathrm{GS_{att}}}$ at the time t^* during the plateau, as sketched in Figure 7.

$$\begin{cases} V_{\mathrm{GS_f}}(t) < V_{\mathrm{GS_att}}(t) & \text{if } 0 < t < t^* \\ V_{\mathrm{GS_f}}(t) > V_{\mathrm{GS_att}}(t) & \text{if } t^* < t < t_3 \end{cases} \tag{17}$$

Figure 7. Principle of the detection of the gate-source plateau.



Assuming V_{GS} as a ramp before the voltage plateau, it can be shown that the filtered voltage $V_{\mathrm{GS_f}}(t)$ can be expressed as:

$$V_{\mathrm{GS_f}}(t) = \begin{cases} \frac{mG}{(s_p)^2}(s_p - s_z)(1 - e^{-s_p \cdot t}) + \frac{mGs_z}{s_p} \cdot t & \text{if } 0 < t < t_2 \\ \frac{mG}{s_p^2}(s_p - s_z)e^{-s_p \cdot t}(e^{s_p \cdot t_2} - 1) + \frac{mGs_z}{s_p} \cdot t_2 & \text{if } t_2 < t < t_3 \end{cases} \tag{18}$$

where

$$m = \frac{V_{TH}}{t_1} \tag{19}$$

$$G = \frac{C_{sm1}}{C_{sm1} + C_{sm2}} \tag{20}$$

$$s_z = \frac{1}{R_{sm1} \cdot C_{sm1}} \tag{21}$$

$$s_p = \frac{R_{sm1} + R_{sm2}}{R_{sm1} \cdot R_{sm2} \cdot (C_{sm1} + C_{sm2})} \tag{22}$$

On the basis of the two considered voltages $V_{\mathrm{GS_f}}$ and $V_{\mathrm{GS_att}}$, it is possible to find out the time t^* during the voltage plateau when they are equal.

$$V_{\mathrm{GS_f}}(t^*)|_{(t_2 < t^* < t_3)} = k_{din_adp} V_{GS_{plateau}} \tag{23}$$

$$\frac{mG}{s_p^2}(s_p - s_z)e^{-s_p \cdot t^*}(e^{s_p \cdot t_2} - 1) + \frac{mGs_z}{s_p} \cdot t_2 = k_{din_adp} V_{GS_{plateau}} \tag{24}$$

$$t^* = -\frac{1}{s_p} \cdot ln\left[\frac{k_{din_adp} V_{GS_{plateau}} - \frac{mGs_z}{s_p} t_2}{\frac{G}{s_p^2}(s_p - s_z)(e^{s_p \cdot t_2} - 1)}\right]. \tag{25}$$

Firstly, a minimum value for C_{sm1} = 200 fF is set and a reasonable value of $R_{sm1} = 62\ k\Omega$ is chosen to set the zero $s_z = 12.8\ MHz$. Consequently, the value of $C_{sm2} = 2.5\ pF$ and $R_{sm2} = 19\ k\Omega$ are set in order to place the pole $s_p = 4.05\ MHz$ before the zero. In this way an instant t^* in the range $[t_2 - t_3]$ according to Equation (25) is found out and a correct trigger event can be provided. As soon as the mentioned two voltages $V_{\mathrm{GS_att}}$ and $V_{\mathrm{GS_f}}$ reach the same value during the gate-source plateau voltage due to the Miller effect, a comparator finds out a trigger event. Such an event enables to write the register whenever the Power MOSFET is in saturation during its switching transient. In the register, the digital value of the SenseFET current I_{MIRROR} is stored. Such a value represents the current to sense I_{unknown} scaled by the mirroring ratio K.

The proposed circuit is suitable for inductor current monitoring in DC-DC converter that operates in Continuous Conduction Mode (CCM) and whenever the detection of the current flowing in a Power MOSFETs operating in PWM that drive resistive and inductive loads is needed. The current to be monitored ranges from $100\ \mu A$ to 5 A, and the mirroring factor K has been set **K** = 10^4. The sensibility of the designed sensor is $50\ \mu A$ (LSB). The absence of the amplifier provides an higher immunity to EMI and a faster response in inductor-current monitoring than the traditional current-sensing technique as shown in Section 5.

5. Prediction of Integrated Current Sensors to RFI

This section shows the results of the time-domain simulations carried out to evaluate the susceptibility of the proposed current sensor and the traditional sensor to RFI.

The proposed new current sensor is based on the transient behavior of the Power MOSFET in which the current to detect flows, and such a transient strongly depends on the parasitics of the Power transistor itself. For this reason, no other additional parasitic capacitances due to the test circuit have to affect the transient behavior of the Power MOSFET. Therefore, a CW RFI current of magnitude $i_{\mathrm{RF}} = 200$ mA has been superimposed onto the current to detect I_{D} by means of a toroidal RF transformer.

In fact, the analyses of the susceptibility to RFI have been carried out referring to the schematic view of Figure 8 similarly to immunity tests [21]. A resistor R_{BIAS} sets the value of the current I_{D}.

Figure 8. Schematic view of the Power MOSFET considered in the time-domain simulations.

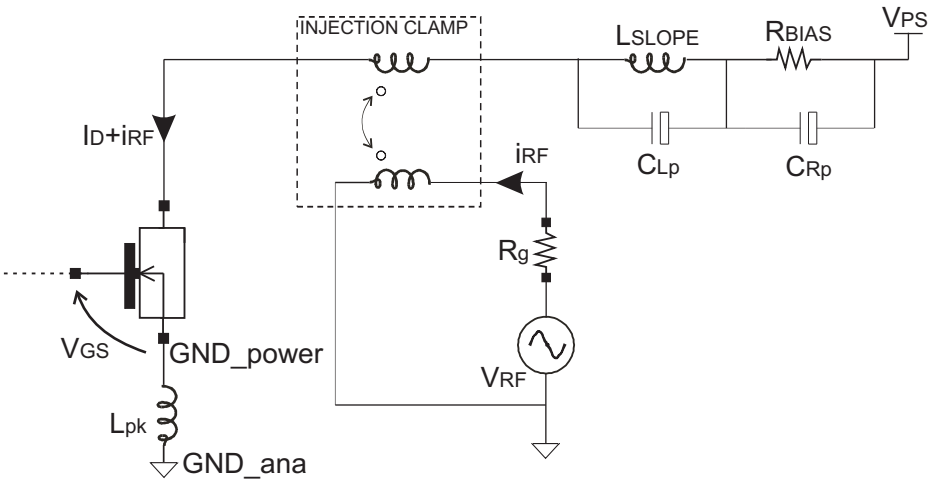


Figure 9 shows the switching transient traces (V_{DS}, V_{GS}) of a Power MOSFET in which the current to be detected I_{D} flows, as well as the respective currents provided by a traditional SenseFET sensor (I_{SENSE}) and the proposed new sensor (I_{MIRROR}). In such a time-domain simulations, a CW RFI current $i_{\mathrm{RF}} = 200\ mA$ at 100 MHz superimposed on the drain current have been considered. The currents provided by the traditional SenseFET sensor (I_{SENSE}) and by the proposed new sensor (I_{MIRROR}) versus current to sense I_{D} and their minimum and maximum errors due to the aforementioned RFI magnitude at 10 MHz, 100 MHz and 400 MHz are shown respectively in Figures 10–12. Furthermore, the minimum and maximum errors of the two considered currents due to a CW RFI $i_{\mathrm{RF}} = 200\ mA$ superimposed on the drain current I_{D} versus frequency are reported in Figure 13. The results highlight that the immunity of the proposed current sensor to RFI is significantly greater than that of the conventional SenseFET circuit shown in Figure 1.

Figure 9. Switching transient traces of a Power MOSFET (V_{DS}, V_{GS}, I_D) and the respective currents provided by a traditional SenseFET sensor (I_{SENSE}) and the new sensor based on the Miller effect (I_{MIRROR}). CW RFI current amplitude 200 mA @ 100 MHz superimposed on the drain current.

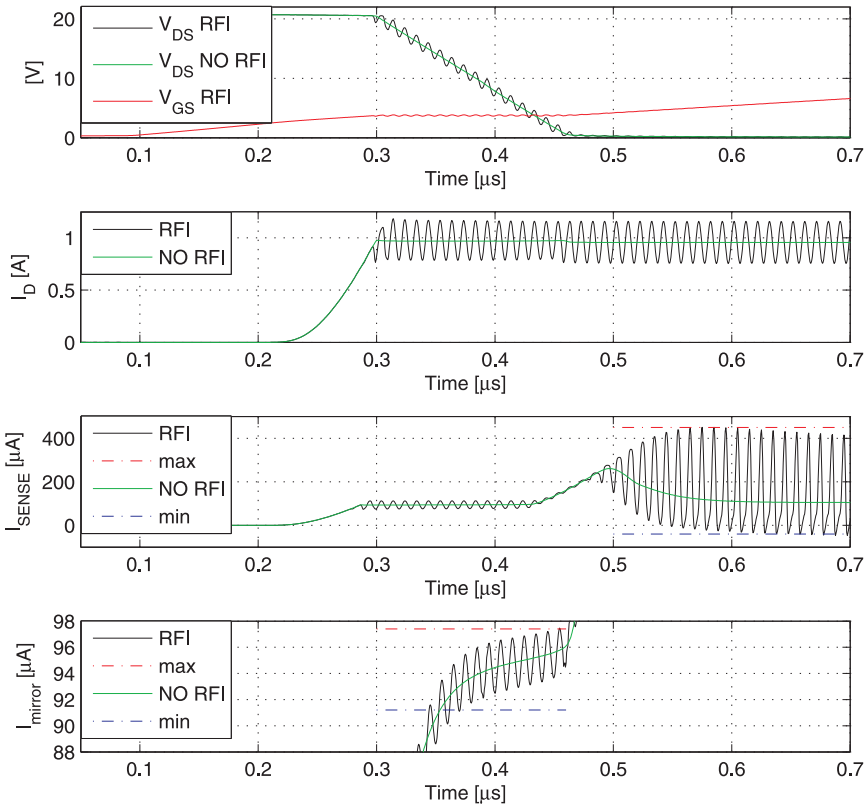


Figure 10. Maximum and minimum current-sensing of the traditional SenseFET current sensor (I_{SENSE}) and the new sensor based on the Miller effect (I_{MIRROR}) *versus* current to sense I_D. CW RFI current amplitude 200 mA @ 10 MHz.

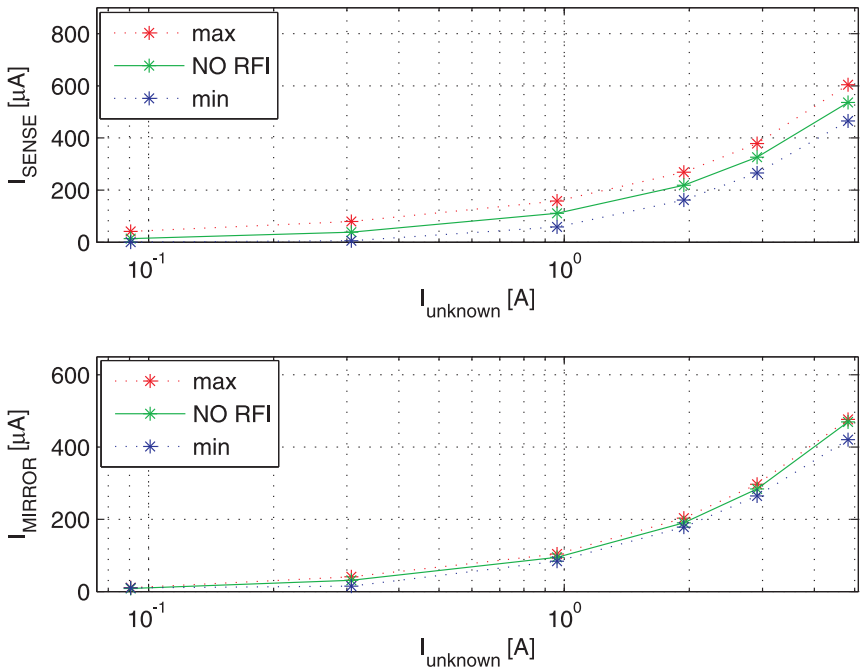


Figure 11. Maximum and minimum current-sensing of the traditional SenseFET current sensor (I_{SENSE}) and the new sensor based on the Miller effect (I_{MIRROR}) *versus* current to sense I_{D}. CW RFI current amplitude 200 mA @ 100 MHz.

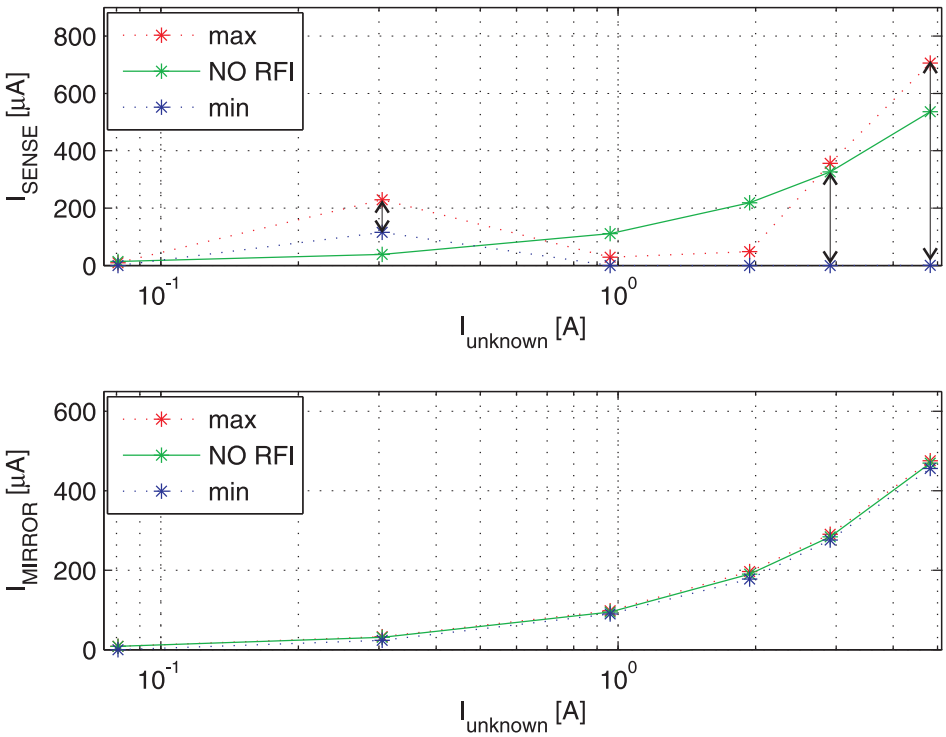


Figure 12. Maximum and minimum current-sensing of the traditional SenseFET current sensor (I_{SENSE}) and the new sensor based on the Miller effect (I_{MIRROR}) *versus* current to sense I_{D}. CW RFI current amplitude 200 mA @ 400 MHz.

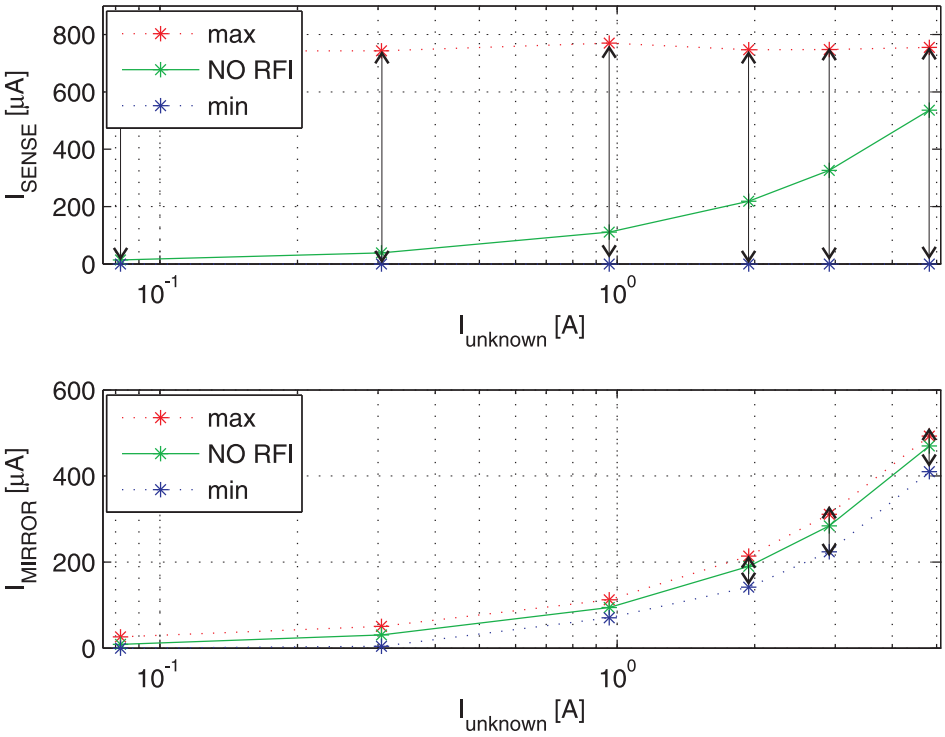
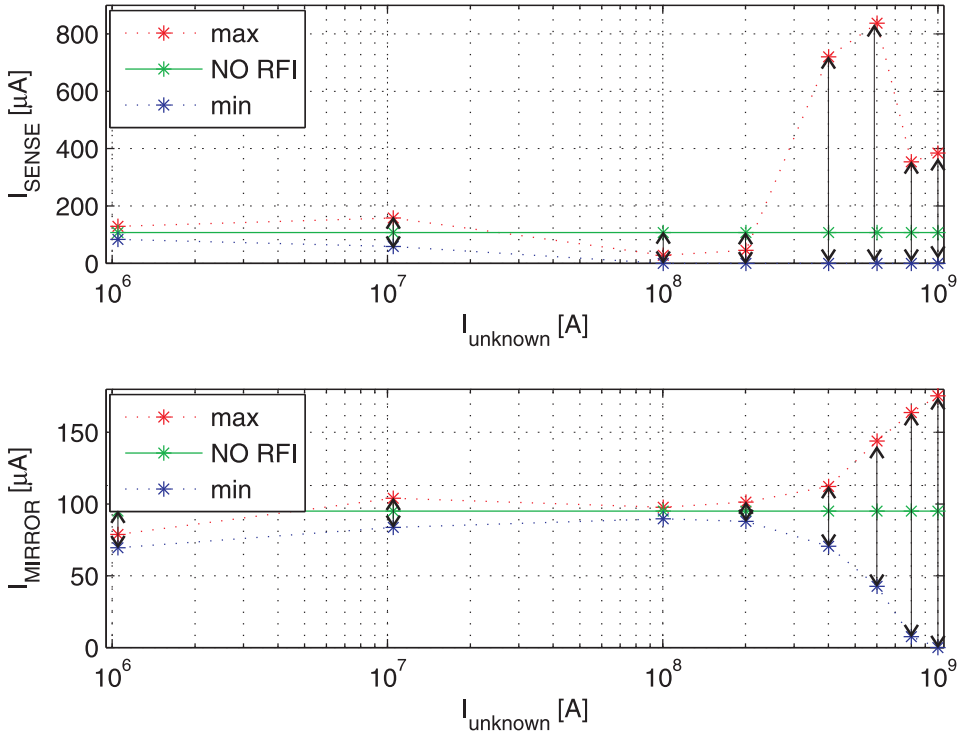


Figure 13. Maximum and minimum current-sensing of the traditional SenseFET current sensor (I_{SENSE}) and the new sensor based on the Miller effect (I_{MIRROR}) *versus* frequency. CW RFI current amplitude 200 mA superimposed on a current $I_{\mathrm{D}} = 1A$.



6. Conclusions

In this work, the susceptibility of common integrated sensors to RFI has been discussed for power transistor current monitoring. In order to improve the immunity of Power MOSFET transistor to RFI in current sensing, a new integrated solution has been proposed. It exploits the Miller effect on the switching transient of the Power MOSFET. The detection of the gate-source voltage plateau due to the Miller effect allows to mirror the current to be detected whenever the Power MOSFET operates in saturation. In this way, the mirrored current is not dependent on the drain-source voltage and the RFI that reaches the drain terminal of the Power MOSFET does not strongly influence the operation of the current sensor. Furthermore, there is no need to connect any amplifier to the drain terminal of the Power MOSFET, hence eliminating a barrier on the overall current sensor performance. The operation of the new current sensing circuit and that of a conventional current sensor have been compared in time-domain simulations. Since the novel sensor operates during the switching transient, it provides a faster current detection than the traditional sensor. Whereas the amplifier usually limits the performance of the SenseFET-technique, no such issue has to be considered for the new sensor. The susceptibility of the proposed current monitoring solution has been evaluated through time-domain simulations and compared with that of a conventional current sensor. The analyses carried out in this work have shown a significant improvement in the immunity to RFI in the range 1 MHz–1 GHz that the new proposed solution enables.

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